



October 2015

FDD7N25LZ

N-Channel UniFET™ MOSFET

250 V, 6.2 A, 550 mΩ



Features

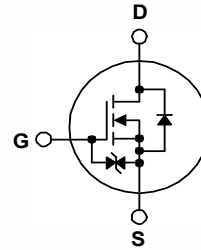
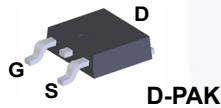
- $R_{DS(on)} = 430 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 3.1 \text{ A}$
- Low Gate Charge (Typ. 12 nC)
- Low C_{rss} (Typ. 8 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Applications

- LCD/LED/PDP TV
- Consumer Appliances
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDD7N25LZTM	Unit
V_{DSS}	Drain to Source Voltage	250	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	6.2
		- Continuous ($T_C = 100^\circ\text{C}$)	3.7
I_{DM}	Drain Current	- Pulsed (Note 1)	25
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	115
I_{AR}	Avalanche Current	(Note 1)	5.5
E_{AR}	Repetitive Avalanche Energy	(Note 1)	5.6
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	10
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	56
		- Derate Above 25°C	0.45
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDD7N25LZTM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.2	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	110	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD7N25LZTM	FDD7N25LZ	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$, $T_C = 25^\circ\text{C}$	250	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.25	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 250 \text{ V}$, $V_{GS} = 0 \text{ V}$ $V_{DS} = 200 \text{ V}$, $T_C = 125^\circ\text{C}$	-	-	1 10	μA
I_{GSSF}	Gate to Body Leakage Current, Forward	$V_{GS} = 20 \text{ V}$, $V_{DS} = 0 \text{ V}$	-	-	10	μA
I_{GSSR}	Gate to Body Leakage Current, Reverse	$V_{GS} = -20 \text{ V}$, $V_{DS} = 0 \text{ V}$	-	-	-10	μA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	1.0	-	2.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 3.1 \text{ A}$ $V_{GS} = 5 \text{ V}$, $I_D = 3.1 \text{ A}$	-	0.43 0.45	0.55 0.57	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}$, $I_D = 3.1 \text{ A}$	-	7	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	480	635	pF
C_{oss}	Output Capacitance		-	65	85	pF
C_{rss}	Reverse Transfer Capacitance		-	8	12	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 250 \text{ V}$, $I_D = 6.2 \text{ A}$, $V_{GS} = 10 \text{ V}$	-	12	16	nC
Q_{gs}	Gate to Source Gate Charge		-	1.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		(Note 4)	-	4	-

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250 \text{ V}$, $I_D = 6.2 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_G = 25 \Omega$	-	10	30	ns
t_r	Turn-On Rise Time		-	15	40	ns
$t_{d(off)}$	Turn-Off Delay Time		-	75	160	ns
t_f	Turn-Off Fall Time		(Note 4)	-	30	70

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	6.2	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	25	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$, $I_{SD} = 6.2 \text{ A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}$, $I_{SD} = 6.2 \text{ A}$	-	130	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100 \text{ A}/\mu\text{s}$	-	0.6	-	μC

Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. $L = 6 \text{ mH}$, $I_{AS} = 6.2 \text{ A}$, $V_{DD} = 50 \text{ V}$, $R_G = 25 \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 6.2 \text{ A}$, $di/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

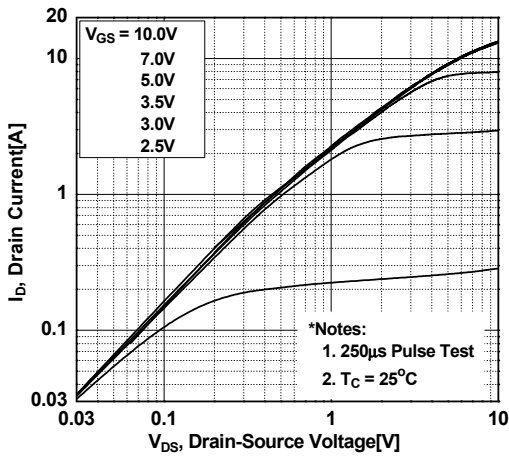


Figure 2. Transfer Characteristics

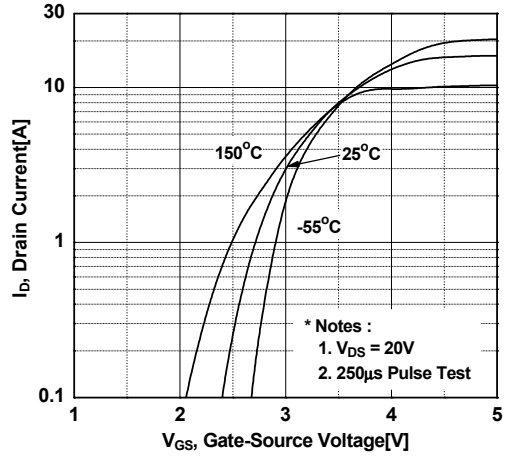


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

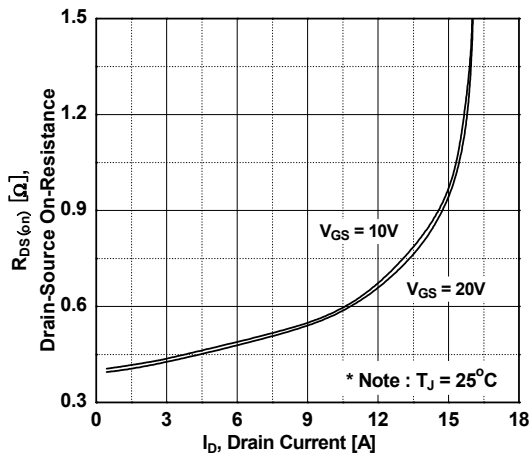


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

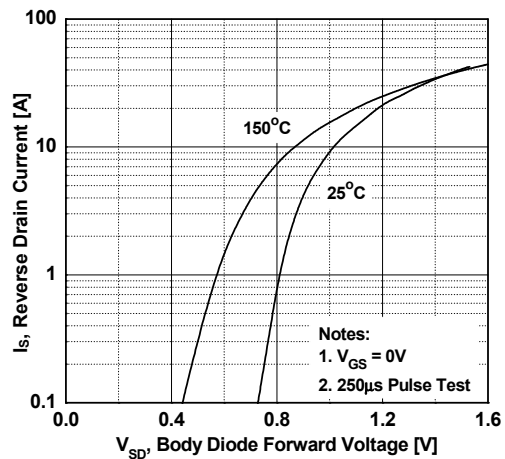


Figure 5. Capacitance Characteristics

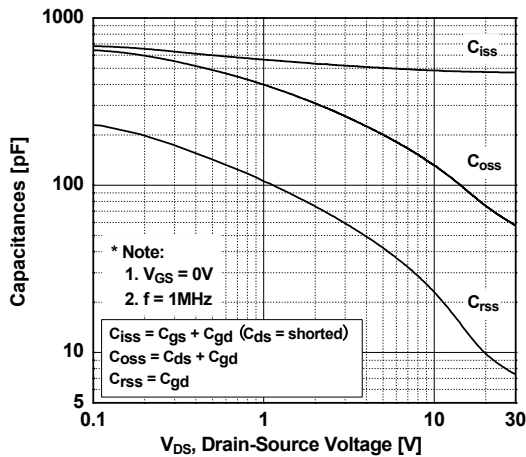
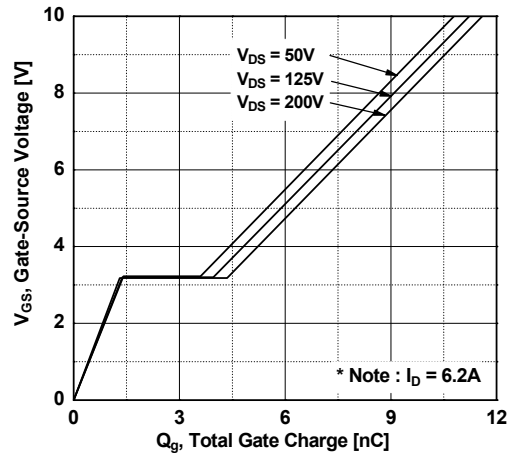


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

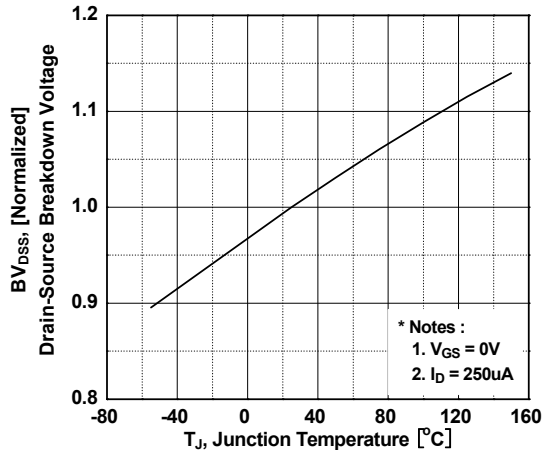


Figure 8. On-Resistance Variation vs. Temperature

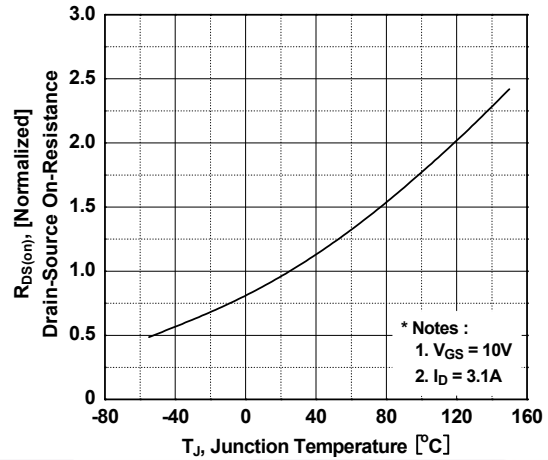


Figure 9. Maximum Safe Operating Area

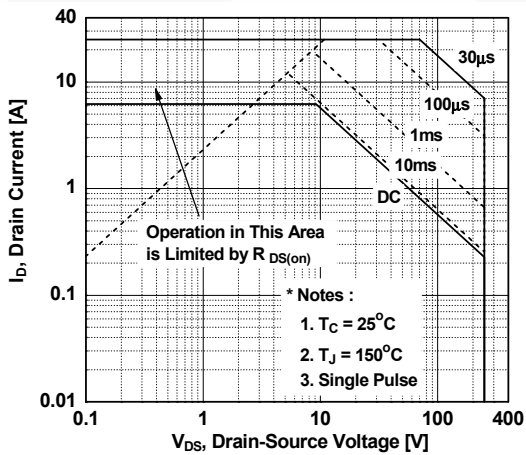


Figure 10. Maximum Drain Current vs. Case Temperature

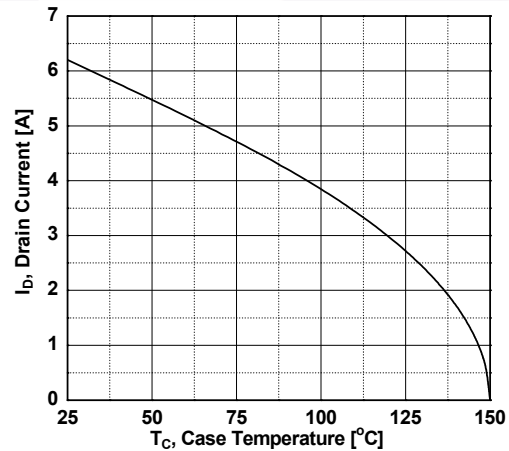


Figure 11. Transient Thermal Response Curve

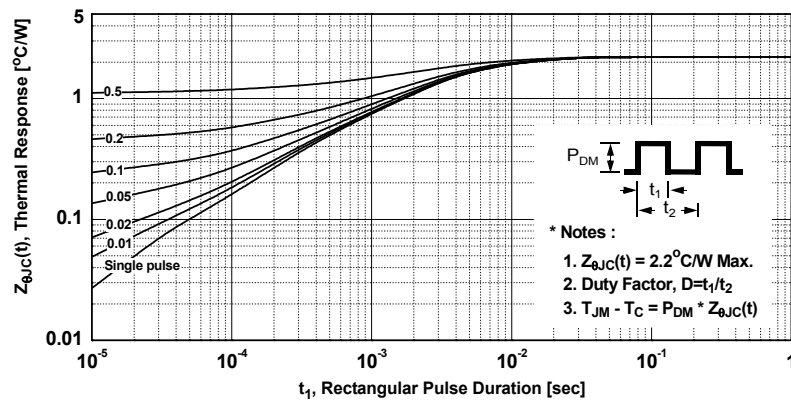




Figure 12. Gate Charge Test Circuit & Waveform



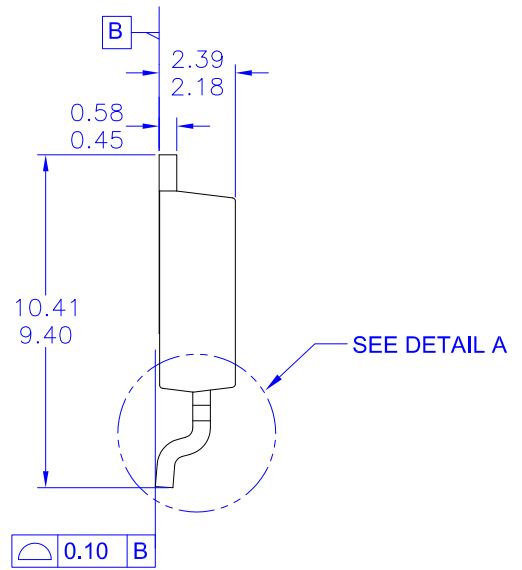
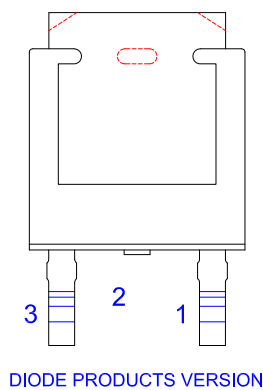
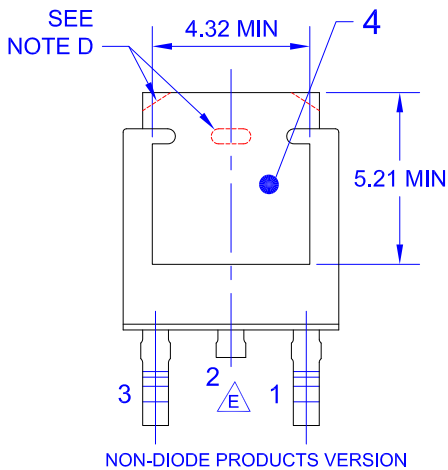
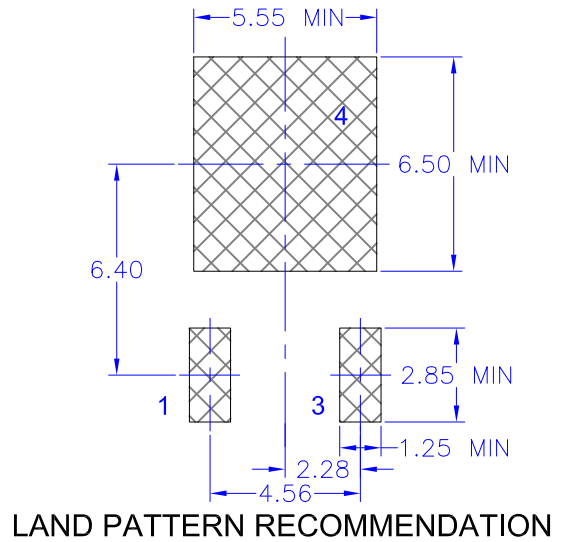
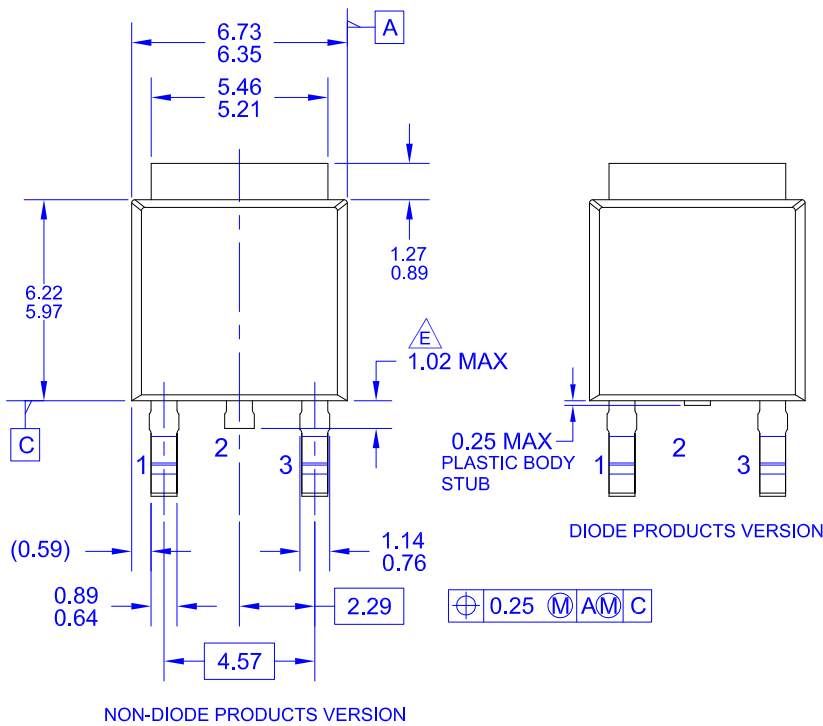
Figure 13. Resistive Switching Test Circuit & Waveforms



Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

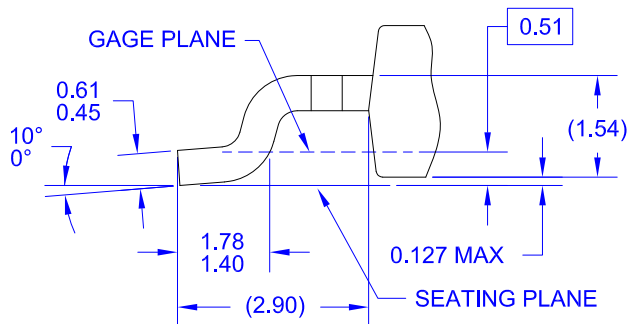


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV10



DETAIL A
(ROTATED -90°)
SCALE: 12X





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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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